Disclosure to Promote the Right To Information

Whereas the Parliament of India has set out to provide a practical regime of right to information for citizens to secure access to information under the control of public authorities, in order to promote transparency and accountability in the working of every public authority, and whereas the attached publication of the Bureau of Indian Standards is of particular interest to the public, particularly disadvantaged communities and those engaged in the pursuit of education and knowledge, the attached public safety standard is made available to promote the timely dissemination of this information in an accurate manner to the public.

"जानने का अधिकार, जीने का अधिकार"
Mazdoor Kisan Shakti Sangathan
"The Right to Information, The Right to Live"

"पुराने को छोड़ नये के तरफ"
Jawaharlal Nehru
"Step Out From the Old to the New"

IS 12350 (1987): Expression of the properties of logic analyzers [LITD 8: Electronic Measuring Instruments, Systems and Accessories]

"ज्ञान से एक नये भारत का निर्माण"
Satyanarayan Gangaram Pitroda
"Invent a New India Using Knowledge"

"ज्ञान एक ऐसा खजाना है जो कभी चुराया नहीं जा सकता है"
Bhartṛhari—Nītiśatakam
"Knowledge is such a treasure which cannot be stolen"

BLANK PAGE

Indian Standard

EXPRESSION OF THE PROPERTIES
OF LOGIC ANALYZERS

National Foreword

This Indian Standard, which is identical with IEC Pub 776 (1983) 'Expression of the properties of logic analyzers', issued by the International Electrotechnical Commission (IEC), was adopted by the Indian Standards Institution on the recommendation of the Electronic Measuring Equipment Sectional Committee and approval of the Electronics and Telecommunication Division Council.

Wherever the words 'International Standard' appear referring to this standard, they shall be read as 'Indian Standard'.

Cross Reference

In this Indian Standard, the following International Standards are referred to. Read in their respective places the following:

International Standard	*Corresponding Indian Standard*
IEC Pub 351-1 (1976) Expression of the properties of cathode-ray oscilloscopes, Part 1 General	IS : 11018 (Part 1)-1984 Expression of the properties of cathode-ray oscilloscopes: Part 1 General (Identical)
IEC Pub 359 Expression of the functional performance of electronic measuirng equipment	IS : 9176-1979 Method for specifying the functional performance of the electronic measuring equipment (Technically equivalent)

The Technical Committee responsible for the preparation of this standard has reviewed the provisions of the following IEC standards and has decided that these are acceptable for use in conjunction with this Indian Standard.

IEC Pub 469-1 (1987) Pulse techniques and apparatus, Part 1 Pulse terms and definitions.

IEC Pub 469-2 (1987) Pulse techniques and apparatus, Part 2 Pulse measurement and analyses, general considerations.

Only the English language text of the International Standard has been retained while adopting it in this Indian Standard.

Electronic Measuring Equipment Sectional Committee, LTDC 21 [Ref : Doc : LTDC 21 (1154)]

As in the Original Standard, this Page is Intentionally Left Blank

1. Scope

This standard applies to logic analyzers as described in Sub-clause 3.1. Only a few test procedures are required to verify the proper operation of a logic analyzer. Features such as triggering capability and data formatting are operations performed internally using digital logic circuitry. Display representation are of pseudo-waveform or formatted word displays; such displays do not require elaborate analogue measurement techniques, as would an oscilloscope display.

This standard does not apply to signature analyzers.

2. Object

To lay down uniform methods of expression of the properties of logic analyzers, and more particularly:

— to define special terminology and catalogue data related to these types of apparatus;

— to specify conditions and methods for testing these types of apparatus in order to verify compliance with properties claimed or specified by the manufacturer.

References

The following publications were used in the preparation of this standard:

— I E C Publication 351-1: Expression of the Properties of Cathode-ray Oscilloscopes, Part 1: General.

— I E C Publication 359: Expression of the Functional Performance of Electronic Measuring Equipment.

— I E C Publication 469-1: Pulse Techniques and Apparatus, Part 1: Pulse Terms and Definitions.

— I E C Publication 469-2: Part 2: Pulse Measurement and Analysis, General Considerations.

SECTION ONE — DEFINITIONS

For the purpose of this standard, the special meanings contained in the following clauses shall apply.

3. General terms

3.1 *Logic analyzer*

An instrument, oriented to hardware and software analysis, used to acquire logic signals in real time with respect to a trigger event, and to represent those signals in various ways. Primary features are the ability to record from a single channel (serial mode) or simultaneously from many channels (parallel mode) and to display signals captured before and/or after the trigger event.

4. Terms related to triggering

4.1 *Trigger event*

An event or sequence of events that controls or references the acquisition of logic signals. The trigger event may originate from internal circuitry, be derived internally from the signal pattern, or be obtained from an external trigger source.

4.2 *Word recognition*

The matching of pre-set word (data pattern) to the presence or absence of that word in the logic signals acquired by the logic analyzer. A trigger event may be generated if word recognition occurs.

4.3 *Don't care*

The condition under which the input signal on a given channel is ignored for the purpose of word recognition.

4.4 *Trigger qualifier*

One or more input channels which serve as an additional condition which must be met simultaneously with an incoming word before word recognition can occur. This signal may be recorded and/or displayed.

4.5 *True trigger*

The condition under which the specified word will cause word recognition.

4.6 *False trigger*

The condition under which any word except the one specified will cause word recognition.

Note. — False trigger is sometimes referred to as "Not". This is the opposite of True trigger.

4.7 *Synchronous word recognition*

A process in which word recognition occurs when the selected word is true at the transition of a clock that is phase-related to that word.

4.8   *Asynchronous word recognition*

A process in which word recognition occurs when the selected word occurs.

4.9   *Glitch*

A pulse narrower than the minimum pulse duration criterion.

4.9.1   *Glitch trigger*

A trigger event is generated if a glitch occurs on one or more operator specified channels.

Note. — A glitch trigger may be used alone or in combination with word recognition.

4.9.2   *Glitch filter*

A means of avoiding triggering on a glitch.

Note. — A word should be present for a minimum selectable interval before word recognition may occur.

4.10   *Sequential triggering*

In sequential triggering, the trigger event is dependent upon a sequence of events.

Note. — The sequence may include word recognition, word count (pass count), clock count (clock delay), time delay, or combinations thereof.

4.11   *OR'd word recognition*

Simultaneous search for two or more events, any one of which can constitute the trigger event.

4.12   *Trigger window*

The upper and lower limits for the range are preselected. The occurrence of any word within the range will constitute a trigger event.

Note. — Trigger window may also be referred to as range trigger.

4.13   *External trigger input*

An input for a trigger signal that is obtained external to the logic analyzer.

4.14   *Manual trigger*

A trigger event caused by a hand-actuated control.

4.15   *Time out*

A pre-set interval after which a trigger event will be forced if one has not already occurred.

5

4.16   *Time in*

A pre-set interval during which a trigger event will not be recognized.

4.17   *Trigger output signal*

A signal, time-related to the trigger event, which is externally available.

4.18   *Pre-trigger*

A triggering mode which stops capturing data when the trigger event occurs.

Note. — Triggering may be sequential (see Sub-clause 4.10).

4.19   *Post-trigger*

A triggering mode which starts capturing data when the trigger event occurs.

Note. — Triggering may be sequential (see Sub-clause 4.10).

5.   Terms related to acquisition

5.1   *Acquisition*

The process by which input logic signals are compared at a discrete instant to a threshold level and recorded.

5.2   *Probe*

An input device, constructed as a separate unit, that transmits the input signal from the circuit under test to the logic analyzer. Probes may be passive or active, single or grouped.

5.3   *Input impedance*

The input impedance is the load presented under operating conditions by the logic analyzer to the signal source.

Note. — The impedance is represented by the values of a resistor and a capacitor, connected in parallel, which produce an equivalent impedance.

5.4   *Maximum input voltage*

5.4.1   *Without degradation*

The voltage beyond which the accuracy of the instrument may be impaired.

5.4.2   *Without damage*

The voltage beyond which the instrument or probe may be damaged.

5.5 *Threshold*

A pre-selected voltage to which input signals are compared.

Note. — Any input voltage that is more positive (or less negative) than the threshold voltage is recorded as a logic high value in memory. Any input voltage that is less positive (or more negative) than the threshold is recorded as a logic low.

5.5.1 *Sensitivity*

Minimum required voltage swing for a signal to be detectable at a specified signal duration (see Figure 1, page 15).

5.5.2 *Dual mode threshold*

A mode in which each channel has two pre-selected thresholds against which input signals may be compared.

5.5.3 *Mixed mode threshold*

Different threshold settings on separate channels or groups of channels.

5.5.4 *Variable threshold*

A threshold voltage which can be set at selected values.

5.5.5 *Threshold range*

All values between the most positive and most negative selectable threshold voltage values.

5.5.6 *Threshold error*

The difference between the actual input comparison voltage and the desired threshold voltage (see Figure 1).

5.6 *Synchronous mode*

A mode in which input logic signals are acquired (sampled) in phase-relation to these same signals.

Note. — Based upon the information available at the threshold detectors, the representation of the signals is stored in memory by what is commonly called the external clock.

5.6.1 *Clock*

A signal used to cause the input signals to be sampled at some instant in time.

5.6.2 *Maximum clock rate*

The maximum valid rate of data acquisition, usually expressed in hertz.

5.6.3 *Set-up time*

The interval during which data shall be present and stable before the clock to ensure that the data will be acquired (see Figure 2. page 15).

Note. — It is possible to have negative values for set-up time.

5.6.4 *Hold time*

The interval during which data shall be present and stable after the clock to ensure that the data will be acquired (see Figure 2).

Note. — It is possible to have negative values for hold time.

5.6.5 *Data qualification*

A means which allows the operator to specify the data to be recorded.

5.6.6 *Clock qualifier*

A means by which data acquisition occurs only if certain external qualifying signals are true at the clock transition.

5 7 *Asynchronous mode*

A mode in which input logic signals are acquired (sampled) independent of the system under test.

Note. — Based upon the information available at the threshold detectors, the representation of the signals is stored in memory by what is commonly called the internal clock.

5.7.1 *Resolution*

The minimum detectable interval between transitions.

Note. — For a single channel the resolution is ±1 sample interval. For two or more channels, this uncertainty is increased by skew.

5.7.2 *Skew*

The time difference between input channels.

5.7.3 *Sample interval*

The interval between subsequent samples.

5.7.4 *Minimum pulse duration*

Minimum pulse duration (MPD) is the narrowest pulse that can be detected with certainty. MPD = (1/clock rate) + k, where k is some specified constant.

5.8 *Memory depth*

The maximum number of sequentially storable words.

5.9 *Memory width*

The number of input channels from which input signals are stored in memory.

Note. — Maximum clock rate, memory depth and memory width may be interdependent.

5.10 *Glitch recognition*

Detection of glitches.

5.10.1 *Glitch latch*

A logic device for capturing glitches in which a detected glitch is treated as a pulse that is one sample interval wide (see Figure 3, page 16).

5.10.2 *Glitch memory*

A separate memory for recording detected glitches.

6. **Terms related to data representation**

6.1 *Data representation*

Processing and presentation of the recorded data in various formats.

Note. — Data could be represented on a cathode-ray tube (CRT) display device which may be built-in or external to the logic analyzer. For terms related to a CRT display, refer to I E C Publication 351-1.

6.2 *Instrument set-up*

Internal set-up information represented simultaneously with other formats, or separately as a menu, or some combination thereof.

6.3 *Timing diagram*

The representation of recorded data states and timing relationships as a pseudo-waveform (see Figure 3).

6.4 *Graphic format*

A two-dimensional representation (XY) of specified data, timing, or other factors.

Note. — A data-domain graph plots state magnitude (Y) as a function of state sequence (X).

6.5 *State table*

A tabular form of representing the logic states of the input data channels at each successive sample.

Note. — The logic states may be represented in binary, octal, hexadecimal, decimal, ISO 7-Bit (ASCII), or mnemonic notation.

6.6 *Map*

A matrix format for presenting logic states so that the user system activity can be identified by unique patterns.

Note. — One map form portrays each stored logic word as a separate dot, with the vertical position of the dot proportional to the most significant half of the word, and the horizontal position proportional to the least significant half of the word.

6.7 *Labels*

Provide information to identify the recorded data.

Note. — For example, channel number, channel group or line number.

6.8 *Compare mode*

A mode in which newly acquired signals stored in memory are compared to a reference memory.

Note. — Differences between the two signals may be displayed or detected.

6.9 *Search mode*

Displays data that matches a search word setting.

6.10 *Cursor*

A marker made as a line or as an intensified zone, data or dot on a representation to identify a specified location.

Note. — A simultaneous readout related to the cursor may also be displayed.

SECTION TWO — GENERAL TEST REQUIREMENTS

7. General

General test conditions and procedures will conform to I E C Publication 359. The following data is based on I E C Publication 359.

8. Statement of limits of errors

8.1 Limits of operating error (which apply under rated operating conditions) shall be stated.

8.2 Limits of intrinsic error (which apply under reference conditions) may be stated. In the absence of a statement, they are considered to be equal to the limits of the operating error.

8.3 Limits of influence error may be stated. It is particularly useful to state these limits when one influence quantity or influencing characteristic causes an important part of the operating error. It may also be of interest to state that certain environmental conditions do not contribute to the operating error.

8.4 Limits of variation may be stated when this standard explicitly permits it.

9. **Performance to be verified and checked**

The tests described in this standard are to be performed in order to verify compliance with the manufacturer's stated data. Test procedures are given in Section Three.

10. **Combinations of mainframe with plug-ins**

When a mainframe can accept one or more plug-in devices, the assembly comprising the given plug-in devices and the mainframe itself is considered as a whole and shall comply with relevant requirements for errors and variations, as stated in the following clauses. When another plug-in device is substituted, the new assembly shall also comply with the relevant requirements for error and variations.

11. **Conditions for test location**

Unless otherwise specified in the standard, the following conditions shall be maintained in the test location:

— temperature within the range of 15 °C to 35 °C;

— relative humidity within the range of 45% to 75%;

— air pressure within the range of 70 kPa to 106 kPa (700 mbar to 1 060 mbar);

— the logic analyzer shall be operated with the rated values of supply voltage and frequency.

Note. — The values indicated above should not be confused with those indicated in Table 1 for reference conditions.

12. **Type tests**

12.1 The tests specified in the following sub-clauses are type tests applicable to logic analyzers which are developed after publication of this standard and are ready for use, that is, with covers and accessories, if necessary, fitted.

12.2 When carrying out type tests, each logic analyzer tested shall be subjected to each of the tests laid down in this standard, as applicable, and also other tests as agreed between manufacturer and user.

12.3 In general, measurements for verification shall be carried out with instruments which do not appreciably (or only calculably) affect the values to be measured. In principle, the errors in measurements made with those instruments should be negligible in comparison with the errors to be determined.

12.4 When the error of the instrument is not negligible, the following rule shall apply:

— if a logic analyzer is claimed to have a limit error $\pm e\%$ for a given performance characteristic and the manufacturer uses for its checking an apparatus resulting in an error of measurement of $\pm n\%$, the error being checked shall remain between the limits $\pm(e - n)\%$;

— likewise, if a user checks the same logic analyzer using another apparatus resulting in an error of measurement of $\pm m\%$, he is not entitled to reject the logic analyzer if its apparent error exceeds the limits of $\pm e\%$, but remains within the limits of $\pm(e + m)\%$.

13. General conditions for test purposes

Tests are carried out under the conditions given in Clauses 14 and 15 below and if agreed between manufacturer and user, under that combination of conditions which may be expected to result in the maximum operating errors.

14. Standard values and ranges of influence quantities

14.1 The reference values or ranges, the rated ranges of use and the limit ranges of operation, storage and transport for all influence quantities shall be stated and shall be selected by the manufacturer from one of the usage Groups I, II or III in Clause 6 of I E C Publication 359. Any exceptions to the values given there shall be explicitly and clearly stated by the manufacturer with an indication that they are exceptions.

14.2 The logic analyzer may correspond to one group of rated ranges of use for environmental conditions and to another group for mains supply conditions, but this shall be clearly stated by the manufacturer.

15. Preparation for tests

Before the tests are performed, the following conditions shall apply:

15.1 Adjustments, if any, shall have been performed according to the manufacturer's instructions.

15.2 Before being switched on, the logic analyzer shall be in equilibrium with the temperature and humidity of the ambient air.

15.3 The logic analyzer shall be operated at the rated value of supply voltage for a period equal to the warm-up time as indicated by the manufacturer.

In the absence of any indication, this period shall be 1 h.

15.4 After the warm-up time, further adjustment may be made by means of the appropriate controls in accordance with the manufacturer's instructions.

16. Particular conditions

The controls shall be set, and signals applied to the input, as indicated at the head of each of the applicable clauses.

When no indication is given for a control setting, the control may be set to any suitable value. Unless otherwise specified, no signal is applied.

17. Reference conditions

For purposes of tests on logic analyzers, a selection of influence quantities and influence characteristics with their reference values and/or ranges is given in Table I. The values have been taken from Clause 6 of I E C Publication 359.

TABLE I

Reference conditions

Influence quantities or influence characteristics	Reference conditions		Tolerance on reference values permitted for testing purposes
	When the reference conditions are indicated	In the absence of indication	
Ambient temperature	20 ˚C, 23 ˚C, 25 ˚C, 27 ˚C	20 ˚C	± 2 ˚C
Ambient air relative humidity	45% to 75%		
Air pressure (altitude)	101.3 kPa (1 013 mbar)		
Supply voltage	Rated value		± 1% for d.c. a.c. r.m.s. ± 2% for a.c. peak
Frequency of a.c. supply	Rated value		± 1%
Waveform of a.c. supply voltage	Sinusoidal		Difference between $\sqrt{2}$ times the r.m.s. value and peak values to within ± 1%
Ripple content of d.c. voltage	Value given by the manufacturer	Negligible	

SECTION THREE — TEST PROCEDURES

In each of the following tests the results shall fall within the range of the manufacturer's stated specification.

18. **Sensitivity**

Refer to Figure 1, page 15 Use an appropriate signal generator and clock signal for synchronous logic analyzers, reduce the peak-to-peak value of the signal just to the joint where data is unreliably acquired. Then increase the signal until data is just reliably acquired. This value is the sensitivity.

Note. — It may be necessary to vary the threshold voltage during this procedure. Also, the sensitivity may be influenced by the frequency of the signal.

19. **Maximum clock rate**

Data that meets the set-up and hold time requirements may be acquired by the logic analyzer up to the maximum clock rate specification. While increasing the frequency of the clock, verify that the data is reliably acquired at clock rates up to the specified maximum. Refer to Clauses 20 and 21 for set-up time and hold time requirements.

20. **Set-up time**

Use appropriate signal generators to obtain signals that match Figure 2, page 30 (for example, two synchronized pulse generators—one having variable delay). While maintaining hold time greater than or equal to hold time specification, vary the set-up time to determine at what value the logic analyzer will no longer acquire the input signal.

21. **Hold time**

Use the same equipment as in Clause 20. While maintaining the set-up time specification, vary the hold time to determine at what value the logic analyzer will no longer acquire the input signal.

22 **Glitch recognition**

Use an appropriate signal generator to obtain a signal to match Figure 3, page 31. While decreasing the pulse duration to the specification of the logic analyzer under test, verify that the glitch is reliably acquired. The pulse shall meet the pulse amplitude requirements.
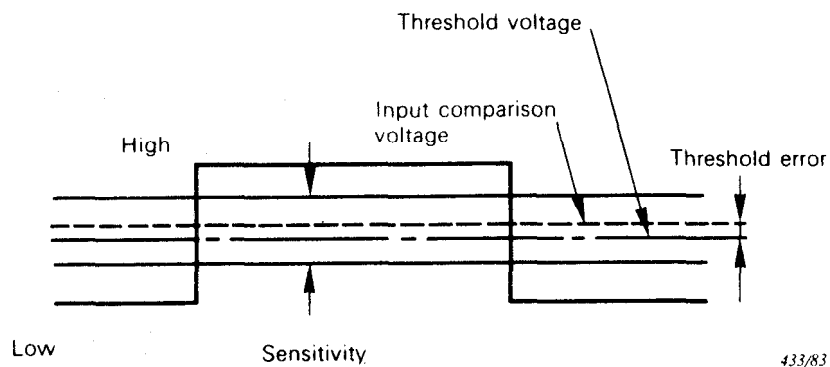
FIG. 1. — Threshold error and sensitivity.
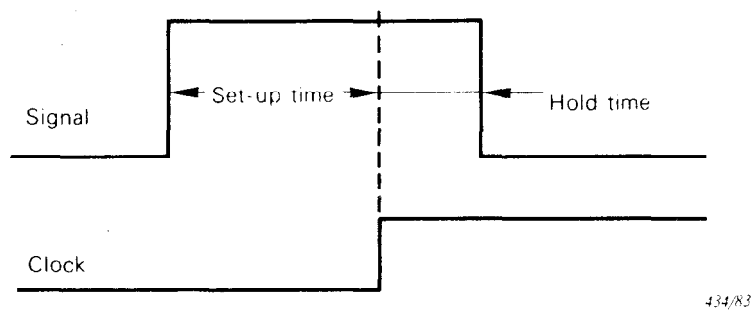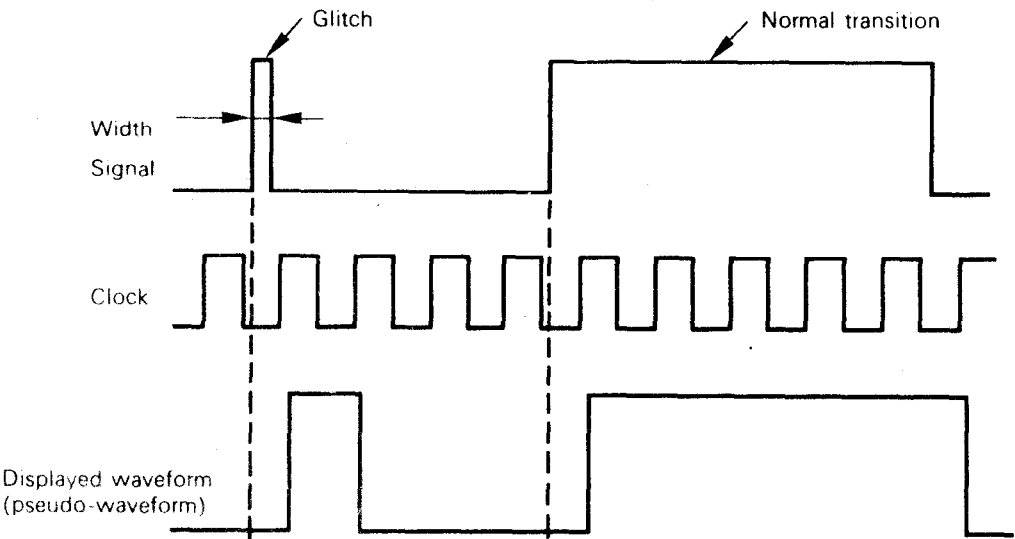

FIG. 2. — Set-up and hold time.

FIG. 3. — Glitch latch.

INDEX OF TERMS